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(54) **Semiconductor device**

(57) An integrated circuit device with a low stress, thin film, protective overcoat having enhanced adhesion both to polymeric materials used in packaging semiconductor devices, and within the passivating film layers, including the following sequence of materials deposited by PECVD processing: a thin film of silicon dioxide, a layer of silicon nitride, oxy-nitride or silicon carbide, and a very thin topmost layer of silicon oxide.

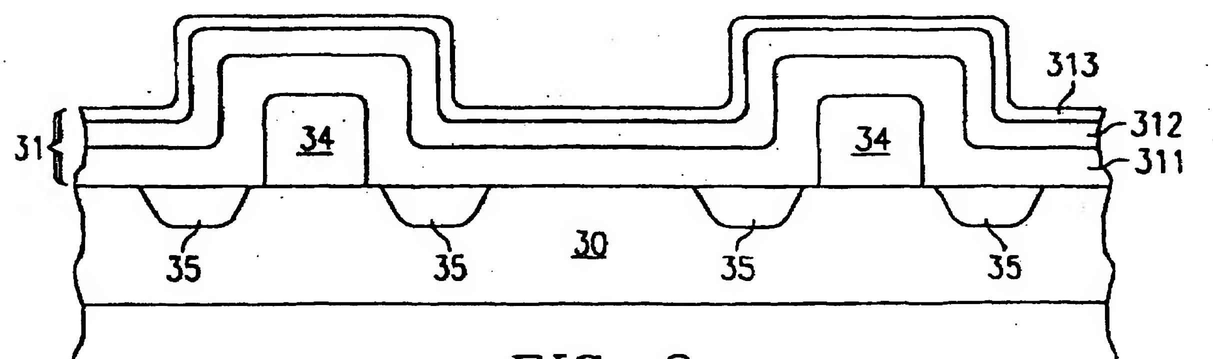


FIG. 3

EP 1 168 437 A2

Descripti n

FIELD OF THE INVENTION

[0001] This invention generally relates to a semiconductor device and more particularly to the protective overcoat on an integrated circuit.

BACKGROUND OF THE INVENTION

[0002] Typically, integrated circuits (IC) are fabricated on a semiconductor substrate, known as a chip, and the most common substrates are made of silicon. The silicon chip is usually assembled into a package which serves to provide effective enlargement of the distance or pitch between input/output contacts of the chip making it suitable for attachment to a printed circuit board, and to protect the IC from mechanical and environmental damage. Unfortunately, the package intended to provide that protection sometimes contributes to the device failure. Such is the case with some surface mount packages housing VLSI chips in which poor adhesion at the interface between chip and molding compound has caused delamination. A rapid increase in vapor pressure at the delaminated interface, resulting from moisture absorbed by the plastic, and the rapid heat of soldering the package to the printed wiring board causes failures manifested as package cracking, bond wire breakage, and other associated stress related failures.

[0003] Recently the semiconductor industry has introduced reduced package sizes, such as those with area array format VS more typical peripheral attach of the input and output (I/O) terminals to a lead frame encapsulated in molded plastic package. These area array assemblies are Chip Scale Packages (CSP)), an example of which is illustrated in Figure 1, wire bonded or flip chip Ball Grid Array (BGA) packages, and Direct Chip attach (DCA) in which the chip is directly attached to the printed circuit board without use of an intermediate package. Often these area array assembles have solder bumps or balls 11 connected by reflowing the solder from the input/output (I/O) contacts of the chip to a substrate or to the Printed Circuit (PC) Board, making both electrical and mechanical connections. Because the materials of the silicon chip 10 and the substrates or PC board 12 have different coefficients of thermal expansion (CTE), stresses are introduced in the solder connection between the rigid, lower CTE chip and the more compliant, higher CTE PC board. Stresses caused by the thermal expansion mismatch occur during solder reflow, and/or as power to the IC is cycled on and off. The stresses frequently result in mechanical failure of one or more solder joints, and in turn cause electrical failure of the product.

[0004] In an attempt to alleviate the solder fatigue failures, and to distribute the thermally induced stresses over a larger area, a polymeric filler or "underfill" encapsulant 15 is introduced in liquid form to surround the solder balls 11, and to fill the cavity between the chip or CSP 10, and th PC board 12. Typically, the underfill is dispensed near the chip edges and flows under the chip and around the solder balls by capillary action. The "underfill" cures to a rigid form via time, temperature, of ultraviolet exposure, or some combination thereof.

[0005] The "underfill" process has a number of drawbacks, including but not limited to the following: air pockets or voids 16 being entrapped under the device which can lead to localized stress concentrations, poor adhesion of the underfill to one or more of the surfaces encountered, and a tedious and time consuming process. The viscous underfill compound, most commonly an epoxy resin with inorganic fillers, is introduced methodically and slowly in an attempt to overcome void formation under the chip resulting from poor wetting to the protective overcoat on the chip, the substrate surface and/or the solder bumps.

[0006] Adhesion between material surfaces and the effects of poor wetting have long been studied; the controlling factors are recognized as cleanliness, surface tension, and topography, as well as the chemistry of the adherents.

[0007] The chip passivation or protective overcoat (PO) of choice for many semiconductor chip manufacturers is silicon nitride, primarily because it has been shown to provide excellent resistance to ingress of mobile ions and contaminants. However, silicon nitride does not provide active sites for adhesion and wetting, and is subject to stress levels which can lead to cracking, and delamination. Stresses vary by deposition techniques, and concerted attempts are made to control the amount of stress, and to provide compressive forces in order to avoid degradation of the chip perfomance and reliability.

[0008] Because of these shortcomings in silicon nitride protective overcoats, the chip manufacturer is frequently forced to apply a patterned film of polyimide atop the protective overcoat. Figures 2a and 2b illustrate a polyimide film 22 on a chip 20. The polyimide film 22 is applied in an attempt to provide improved adhesion to polymers used in semiconductor packaging, such as molding compounds 26 in a conventional leaded plastic molded package in Figure 2b, or to an underfill or potting compound in other types of packages. The polyimide 22 is applied and patterned atop the silicon nitride or other thin film PO (21).

[0009] Figure 2a provides a more detailed view of the surface topography of a chip 20 with a polyimide film 22 patterned over the protective overcoat 21. With respect to adhesion, the polyimide film may have a negative effect if it is sufficiently thick enough to leave a smooth, planar surface. The thin silicon nitride protective overcoat 21 follows the contours of the chip circuitry 24, but the thicker polyimide 22 softens the contours, making a more level surface; such a smooth surface is not ideally suited to optimum adhesion.

[0010] Further, while the elastic modulus of polyimide

films is higher than typical inorganic films, the thick film coupled with higher th rmal expansion does lead to stress on the wafer which can result in warping and/or delamination. Organic films, such as polyimide have neither the desirable high thermal stability, nor the greater thermal conductivity of inorganic films.

[0011] Polyimide precursors are applied in liquid form to the surface of a wafer having previously been prepared with an adhesion promoter, or alternately having such a compound included in the polyimide formulation. The polyimide must then be photopatterned. The polyimide formulation may include a photosensitive agent which allows direct patterning, or if it does not, a separate photoresist step is required. Next the film is cured or cross linked by a thermal process. Not only is the polyimide a very expensive compound, but the processing is time consuming, costly, and may negatively impact yield of good chips on the wafer.

[0012] Accordingly, a need exists in the industry for a reliable, chip protective overcoat readily wet by, and having good adhesion to polymers, such as molding and underfill compounds, an overcoat which imparts little stress on the chip circuitry, and one which is cost effective in wafer processing.

SUMMARY OF THE INVENTION

[0013] The current invention provides a reliable and cost effective chip protective overcoat having good adhesion between the layers, as well as good wetting and adhesion to polymeric materials used in assembly of integrated circuit chips.

[0014] This invention further provides a manufacturing method for a protective overcoat having enhanced adhesion, and which utilizes existing wafer fabrication equipment and materials.

[0015] This invention yet further provides a thermally stable chip protective overcoat which imparts only small and controllable stresses to the active circuits and metallization on the chip.

[0016] The invention also provides a chip protective overcoat having excellent diffusion barrier properties.

[0017] The invention additionally provides an inorganic chip protective overcoat having improved thermal conductivity as compared to polymeric coatings.

[0018] The invention provides a protective overcoat on an integrated circuit device including the following sequence of materials: a thin film of silicon oxide preferably in the range of 5,000 to 10,000 angstroms thickness over the active circuit and metallization, a layer of silicon nitride, silicon oxy-nitride or silicon carbide of preferably about 1,000 to 5,000 angstroms thickness, and a top adhesion layer of silicon oxide preferably in the range of 500 to 5,000 angstroms thickness. This composite overcoat is preferably fabricated by plasma enhanced chemical vapor deposition onto silicon wafers by changing the gas compositions, and process variables in a reactor, but without additional wafer handling. Openings for input/output terminals are photopatterned and tched in the d posited overcoat layers.

[0019] The first and third layers of silicon dioxide function to control stresses imparted by the nitride, to provide excellent dielectric properties, and to allow adhesion both between the overcoat layers, and to polymers used in assembly of semiconductor devices. The second layer of a silicon nitride, carbide, or oxy-nitride film is used as a barrier against ingress of mobile ions or contaminants.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] Preferred and exemplary embodiments of the present invention will herein after be described in detail by way of example only, with reference to the figures in the accompanying drawings in which:

Figure 1 is a Chip Scale Package with underfill encapsulant. (Prior art)

Figure 2a illustrates a chip surface having a polyimide adhesion layer over protective overcoat. (Prior art)

Figure 2b Is a leaded plastic package housing a semiconductor device with polyimide coating. (Prior art)

Figure 3 shows the successive protective overcoat layers of current invention.

Figure 4 illustrates the process flow for the enhanced adhesion protective overcoat of the current invention.

Figure 5 is a flip chip assemblage having enhanced adhesion between PO and the underfill material.

Figure 6 is a molded semiconductor device of the current invention.

DETAILED DESCRIPTION OF THE DRAWINGS

[0021] Figure 3 provides a cross sectional view of a portion of a semiconductor chip 30 having the protective overcoat structure 31 of the current invention. A number of novel features contribute to a reliable, high performance device having good adhesion both between the multiple dielectric layers of the protective overcoat, and to polymeric materials used in packaging the chip. In Figure 3, device circuitry including metal interconnect lines 34, and buried structures 35 are covered by a passivation or protective overcoat (PO) 31 including the following thin film layers formed in succession; a film of silicon dioxide 311, a second dielectric layer 312 of a silicon compound, preferably silicon nitride, or alternately silicon oxy-nitride or carbide, and a very thin final or topmost layer of silicon dioxide 313. The layers are patterned with openings as required for external contact or other device requirements (not shown).

[0022] Dielectric material layers usually function to provide electric insulation between conductive layers, and to protect underlying structures of the integrated cir-

cuit against contaminants. Additionally, the provision of successive layers ensures protection for the device even when any one of the layers b com s damaged, e. g., by th formation of small cracks. Therefore, it is important that no regions be allowed to have less than perfect adhesion between the overlaid layers.

[0023] The first layer 311 is silicon dioxide in the range of 5,000 to 10,000 angstroms thickness. The term silicon dioxide refers to a not strictly stoichiometric silicon oxide, i.e., Si[x]O[2-x]. This layer serves both to mitigate stresses of the silicon nitride, or second layer of the protective overcoat structure 31, and to provide an excellent dielectric passivation for the device circuitry. The silicon dioxide as both the first 311 and third 313 layers provide adhesion to the middle or barrier 312 layer. Further, the first layer of silicon dioxide imparts little to no tensile stress on the circuitry or metallization of the chip, and serves to decouple stress from the silicon nitride layer to the underlying circuitry.

[0024] In a preferred embodiment, a silicon nitride or barrier layer 312 provides excellent protection against mobile ions, moisture and other contaminants, which in combination with the oxide layers 311, 313 is equal to thicker nitride overcoats of existing technology. In the current invention, a thickness of 1,000 to 5,000 angstroms is adequate for the barrier or second layer.

[0025] In a second embodiment, the second layer of the protective overcoat 312 is a silicon oxy-nitride, and in yet a third embodiment, the second layer is silicon carbide. Oxy-nitrides are preferable in specific device types where selected light transmission is necessary. Silicon carbide is well known for having very high thermal conductivity, and as a PO layer serves both to spread localized heat generated by the circuits across the surface of the chip, and to provide a means to transport heat away from the circuits to the outside world. Techniques have been developed for providing thin'films of silicon carbide which have both excellent barrier characteristics, and the stresses are readily controllable by the deposition parameters.

[0026] The silicon compounds selected for the second or barrier layer refer not strictly to stoichiometric formulations, but instead to mixtures comprising substantially the stated compound, and the mixture as understood within the industry.

[0027] The third or topmost oxide layer is key to adhesion of the overcoat to polymeric materials. Only a very thin film of oxide, in the range of 500 to 5,000 angstroms is required to provide active sites for adhesion to the underlying nitride, and to provide an exposed surface having low surface tension and active sites for wetting and adhesion to polymers and oxides of silicon, such as epoxies used in underfill and plastic molding compounds. Oxides of silicon, e.g., Si-O_x, Si-OH and silane reaction products in various forms are well recognized by those skilled in the art as adhesion promoters for polymers such as epoxies used in underfill and plastic molding compounds as discussed in US Patent 5,795,821 and US Pat nt 5,418,189.

[0028] As previously noted, controlling factors for wetting and adhesion between materials ar recognized as cleanliness, surface tension, and topography, as well as the chemistry of the adherents.

[0029] From Figure 3, it can be noted that the thin film enhanced adhesion overcoat 31 follows the topography of the underlying circuit structures, thereby providing an exposed surface having an irregular texture. It has long been recognized that adhesion is enhanced by a rough or textured surface, as opposed to a smooth, planar surface.

[0030] A significant advantage of the adhesion enhanced protective overcoat is afforded by compatibility of the process with known wafer processing technology, and automation used throughout the industry. Figures 4a through 4d illustrate the steps for fabrication of an overcoat 31, such as that illustrated in Figure 3. In Figure 4a a silicon wafer 40 having 'integrated circuits 44 patterned, including the topmost metal interconnection 45 level are positioned in a plasma enhanced chemical vapor deposition chamber. Using a standard PETEOS (plasma enhanced tetra ethyl ortho silicate) process designated by arrows 401, an oxide film 411 in the range of 5,000 to 10,000 angstroms thick is deposited. In a more detailed view in Figure 4b, the gas source is changed to include silane and nitrogen and/or ammonia with the PECVD process designated by arrows 402 to deposit a film of silicon nitride 412 in the range of 1,000 to 5,000 angstroms thick. The nitrogen sources are removed, and in Figure 4c a final thin layer of oxide 413 is added using a standard PETEOS process 401. The wafer is removed from the chamber, photoresist 403 is applied and photopatterned to expose bond pads 48 and/or other openings required by the device. The pattern is preferably etched using a gaseous dry etching process 404 to remove the protective overcoat layers from the bond pads, and other openings on the device. Alternately, wet etching with buffered hydrofluoric acid is used to etch the PO.

[0031] Fabrication of the second embodiment, a device having protective overcoat layers of silicon dioxide, silicon oxy-nitride, and silicon dioxide differs from that described above in that oxygen is introduced along with nitrogen, silane, and ammonia during the deposition process for the second layer. The processes for silicon oxy-nitride are known and used throughout the industry, in particular for E-PROM devices. Processes for the first and third layers of the overcoat are unchanged from that described above.

[0032] Fabrication of protective overcoat of the third embodiment including a layer of silicon dioxide, silicon carbide, and silicon dioxide differs from the first embodiment in that silane/methane, trimethylsilane, tetramethylsilane, or other organosilane gas is the source gas, along with Ar or He as a carrier gas, for the second layer of silicon carbide. Again the first and third layers are of silicon dioxide using the PETEOS process.

[0033] Each of the processes for deposition and patterning is well known throughout the semiconductor industry, and the equipment is widely used. The combined successive processes form a unique PO structure having enhanced adhesion to polymers used in IC package assembly, as well as good adhesion between the film layers, and having minimal stresses on the circuits, thereby providing a strong, low defect, chip passivation.

[0034] Plasma enhanced chemical vapor deposition (PECVD) of successive overcoat layers eliminates excessive wafer handling by sequentially depositing layered films in a single chamber. Processes employing plasma enhanced chemical vapor deposition provide clean, uncontaminated surfaces between the layers as a function of the atmospheric control within the chamber, thus facilitating adhesion between the multiple layers. Further, PECVD optimizes process cycle time by successive depositions without handling, and by a single photopatterning step to etch openings.

[0035] The completely inorganic overcoat of the cur r nt invention not only provides device performance advantages of enhanced adhesion to packaging polymers, but also has very high temperature stability, in excess of 450 degrees C, and has improved thermal conductivity as compared to existing enhanced surface adhesion PO technology. In particular the embodiment having a silicon carbide second or barrier layer provides good thermal conductivity, and is applicable to high power circuits.

[0036] Figure 5 illustrates a flip chip assemblage of the current invention. An integrated circuit device 50 having sequentially deposited protective overcoat of silicon dioxide 511, silicon nitride 512, and silicon dioxide 513 is attached to a substrate 52 using solder balls 53. A polymeric underfill compound 55 is completely wetted to the oxide surface 513 of the protective overcoat, and no voids resulting from poor adhesion are present in the underfill.

[0037] An alternate embodiment is illustrated in Figure 6 in a cross sectional view of a leaded plastic molded package, wherein the multilayer protective overcoat 61 of the current invention has enhanced adhesion to the molding compound 65. This adhesion is particularly advantageous at the corners of chip 69 where delamination of the plastic can cause shearing of the chip metal structures and /or fatigue of the bond wires.

[0038] While the invention has been described in connection with several preferred embodiments, it is not intended to limit the scope of the invention to a particular form set forth, but on the contrary, it is intended to cover alternatives, modifications and equivalents as may be included within the spirit and scope of the invention.

Claims

1. An integrated circuit having an enhanced adhesion protective overcoat, said overcoat comprising the following thin film layers:

   a first layer of silicon dioxide,
   a second layer a silicon compound selected from a group consisting of silicon nitride, silicon carbide, or silicon oxynitride, and
   a third layer comprising a very thin film of silicon dioxide.

2. An integrated circuit as claimed in claim 1, wherein said first layer has a thickness in the range of 5,000 to 10,000 angstroms.

3. An integrated circuit as claimed in claim 1 or claim 2, wherein said second layer has a thickness range of 1,000 to 5,000 angstroms.

4. An integrated circuit as claimed in any of claim 1 to 3, wherein said third layer has a thickness in the range of 500 to 5,000 angstroms.

5. An integrated circuit as claimed in any preceding claim, wherein each of said layers is deposited by plasma enhanced chemical vapor deposition.

6. An integrated circuit as claimed in any preceding claim, wherein said third layer has strong adhesion to polymeric materials.

7. An integrated circuit as claimed in any preceding claim, wherein said overcoat is thermally stable to a temperature greater than 450 degrees C.

8. An integrated circuit as claimed in any preceding claim, wherein said protective overcoat is a barrier against ingress of moisture, mobile ions, and other contaminants.

9. An integrated circuit as claimed in any preceding claim, wherein said first and third oxide layers have strong adhesion to said second dielectric layer.

10. A passivating film comprising the following thin film layers:

    a first layer of silicon dioxide,
    a second layer of a silicon compound selected from the group consisting of silicon nitride, silicon oxy-nitride, or silicon carbide.

11. A flip chip semiconductor device having a protective overcoat with enhanced adhesion to polymeric materials comprising:

    an integrated circuit having a first surface with active circuits and interconnections,
    a protective overcoat deposited and patterned atop said first surface comprising a first layer of

silicon dioxide, a second dielectric layer comprising a silicon compound, selected from the group consisting of silicon nitride, silicon carbide or silicon oxynitride, and a thin layer of silicon dioxide,
an underfill polymer, and
a substrate with solder ball contacts.

12. A semiconductor device as claimed in claim 11, wherein said device is a BGA package.

13. A semiconductor device as claimed in claim 11, wherein said device is a CSP.

14. A leaded surface mount semiconductor device having a protective overcoat with enhanced adhesion to polymeric materials comprising;

an integrated circuit having a first surface with active circuits and interconnection and a second surface attached to a lead frame,
a protective overcoat deposited and patterned atop said first surface, said overcoat comprising a first layer of silicon dioxide, a second dielectric layer comprising a silicon compound selected from the group consisting of silicon nitride, silicon carbide or silicon oxy-nitride, and a thin, third layer of silicon dioxide,
wire bonds connecting bond pads on the chip to the lead frame, and
a molding compound comprising an epoxy polymer encapsulating said integrated circuit chip with enhanced adhesion protective overcoat, bond wires and the inner leads of a lead frame.

15. A method of forming a semiconductor device having a protective overcoat with enhanced adhesion both to polymeric materials used in packaging and between the layers of said overcoat, the method includes the following steps:

positioning one or more semiconductor wafers including fabricated integrated circuits into a plasma deposition reactor, evacuating the chamber prior to deposition of a silicon dioxide layer using a PETEOS (plasma enhanced tetraethyl ortho silicate) process,
changing gas supply to include a silane, nitrogen and ammonia, using a PECVD (plasma enhanced chemical vapor deposition) process depositing a layer of silicon nitride, changing the gas supply to deposit a thin film of silicon dioxide using a PETEOS process,
applying a photoresist, photopatterning the bond pads and/or other opening, and etching the openings in the protective overcoat using a dry etch process.

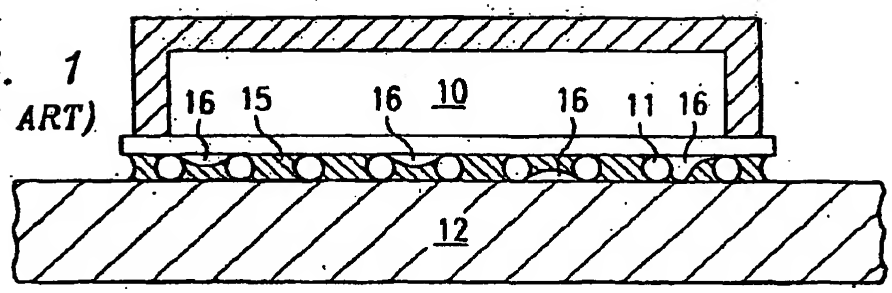
16. A method of forming a semiconductor devic having a protective overcoat with enhanced adhesion both to polymeric materials used in packaging and between the layers of said overcoat, the method includes the following steps:

positioning one or more semiconductor wafers with fabricated integrated circuits into a plasma deposition reactor,
evacuating the chamber prior to deposition of a silicon dioxide layer using a PETEOS (plasma enhanced tetraethyl ortho silicate) process, changing gas supply to include a silane, nitrogen, oxygen and ammonia, using a PECVD (plasma enhanced chemical vapor deposition) process depositing a layer of silicon oxy-nitride, changing the gas supply to deposit a thin film of silicon dioxide using a PETEOS process,
applying a photoresist, photopatterning the bond pads and/or other opening, and etching the openings in the protective overcoat using a dry etch process.

17. A method of forming a semiconductor device having a protective overcoat with enhanced adhesion both to polymeric materials used in packaging and between the layers of said overcoat, the method includes the following steps; evacuating the chamber prior to deposition of a silicon dioxide layer using a PETEOS (plasma enhanced tetraethyl ortho silicate) process, changing gas supply to include silane/methane, or an organosilane, such as trimethyl or tetramethyl silane, using a PECVD (plasma enhanced chemical vapor deposition) process depositing a layer of silicon carbide,

changing the gas supply to deposit a thin film of silicon dioxide using a PETEOS process,
applying a photoresist, photopatterning the bond pads and/or other opening, and etching the openings in the protective overcoat using a dry etch process.

FIG. 1
(PRIOR ART)



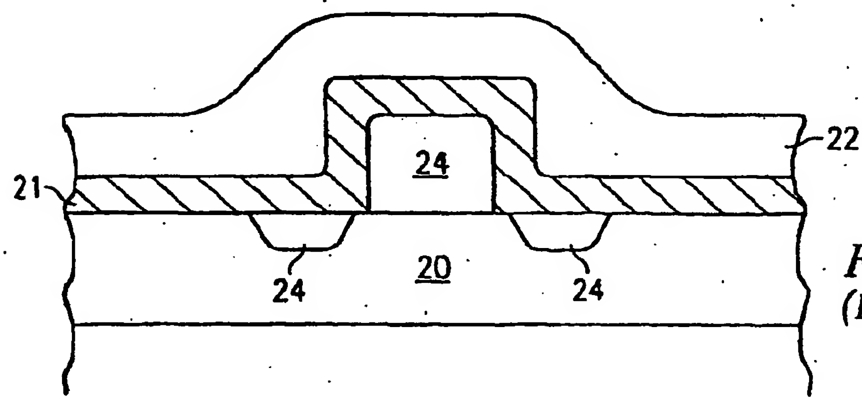
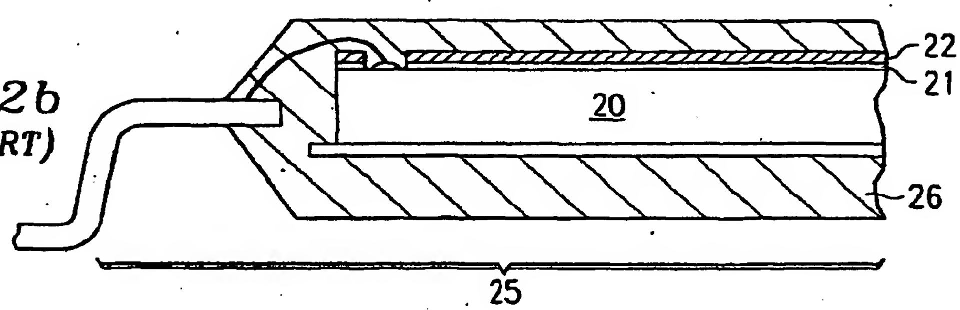


FIG. 2a
(PRIOR ART)

FIG. 2b
(PRIOR ART)



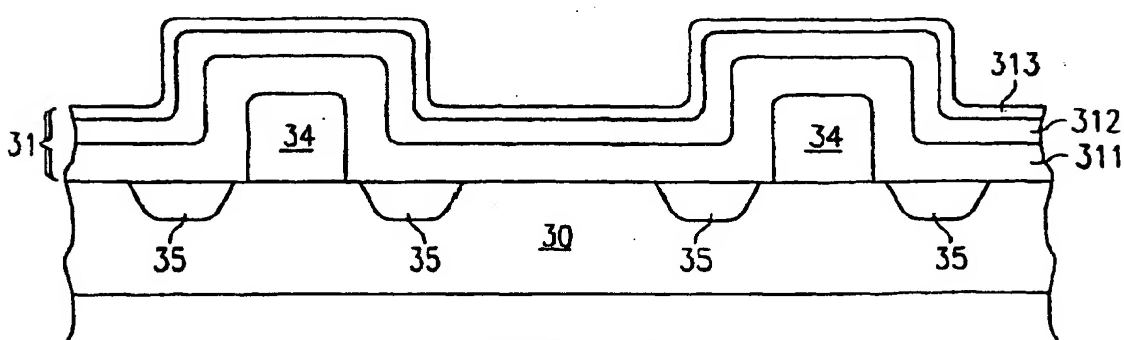


FIG. 3

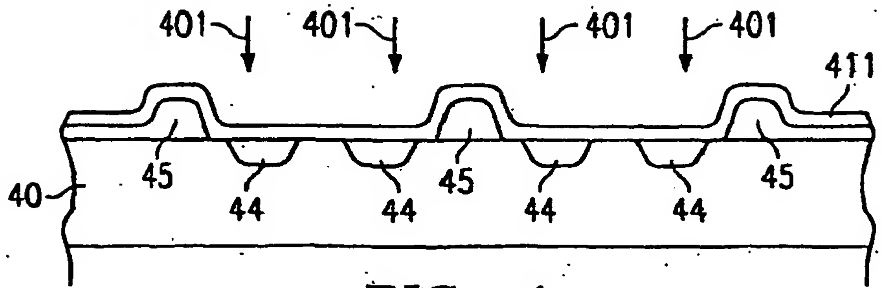


FIG. 4a

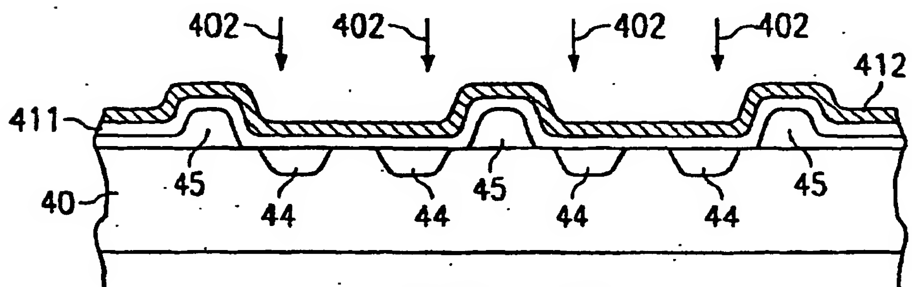


FIG. 4b

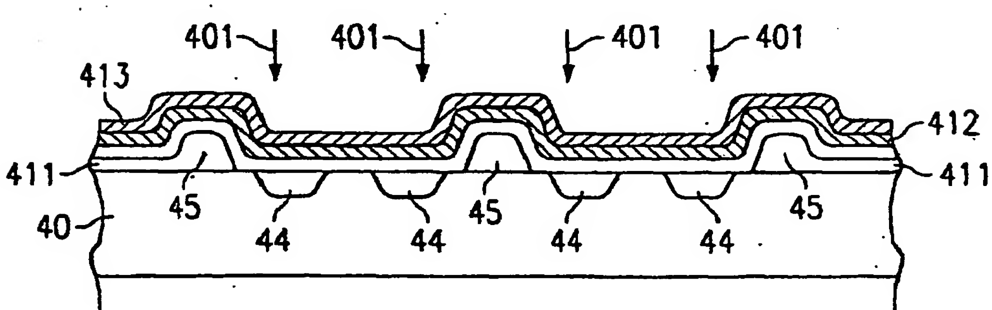


FIG. 4c

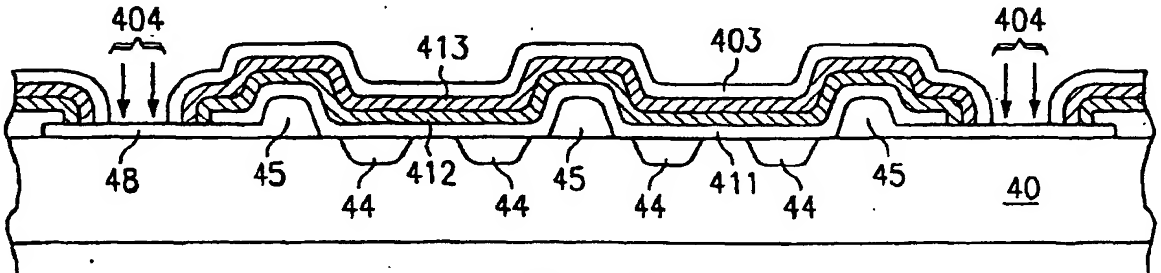


FIG. 4d

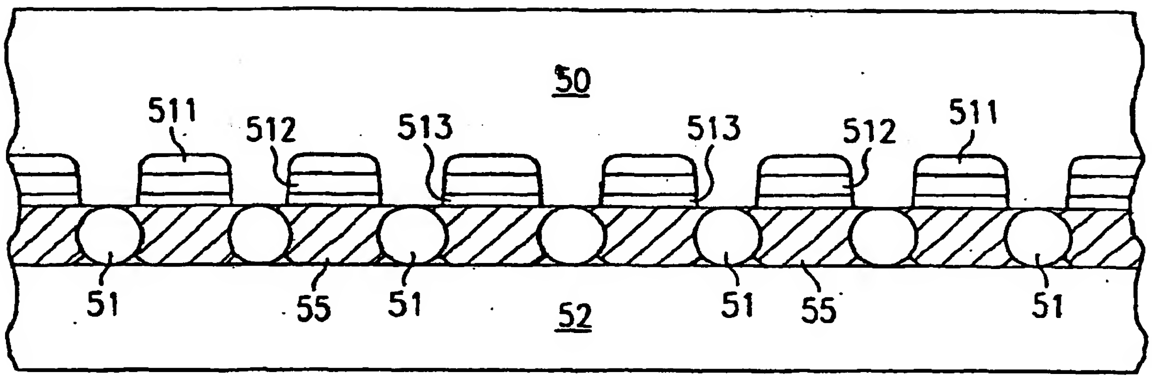


FIG. 5

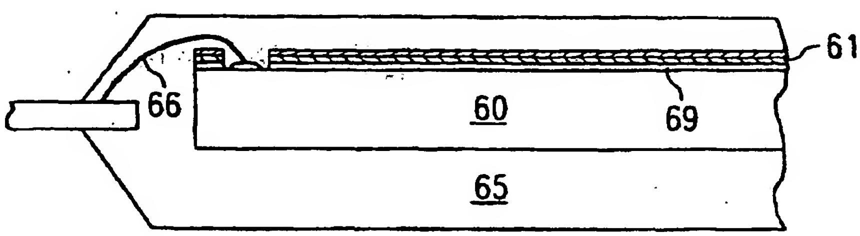


FIG. 6